The World's Shortest Primer on How to Evaluate a PTI

By Roger Sinsheimer

Introduction

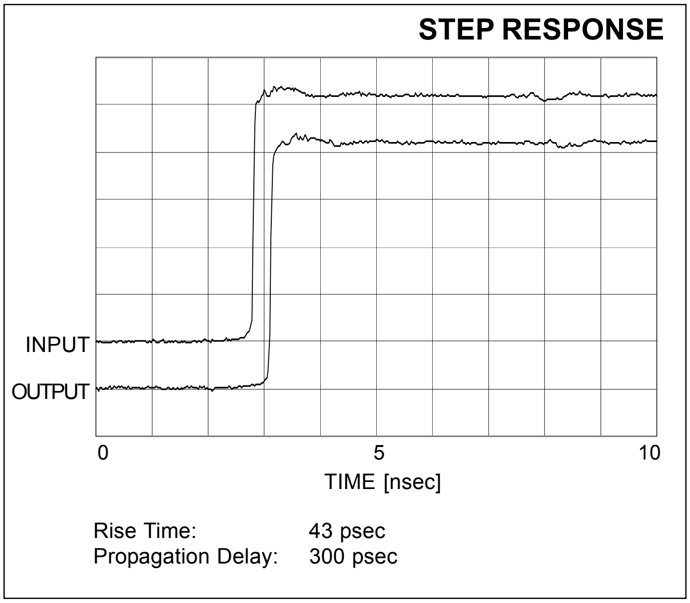
To evaluate the digital signal transmission capabilities of a Prober-Tester-Interface (aka: "PTI," "tower", "Pogo™ stack" or "top hat"), three types of test charts must be created and evaluated:

- Step Response
- Frequency Response
- Reflection Coefficient (Return Loss)

Step Response

Using calibrated, impedance-matched hardware, a fast rising voltage step is injected into the PTI and the resulting signal is captured at the other side. The three most important things to look for in this graph are:

1. Transition time (T_T) or Rise Time (τ): This is the time it takes for the signal to make the transition from 10% to 90% of the full step*. This value is the starting point for evaluating an interface. It is intimately connected to the Bandwidth of the Prober Tester Interface, which will be discussed below. The Transition Time of the interface must be shorter than that of the tester. For example, if the PTI's transition time is 1/7th that of the tester, the resulting degradation will be only 1%. If the PTI's transition time is equal to that of the tester, the combined transition time will increase 41% (see the chart). Note that the τ value accompanying the Step Response graph is corrected for the finite transition time of the test equipment. Also note that the graph itself is *not* corrected, but instead shows the raw data.



Rise Time: 43 psec
Propagation Delay: 300 psec

2. The settling characteristics at the end of the transition (at the "knee" of the curve): Is there evidence of ringing and/or overshoot? What one generally expects to see is a rounding of this portion of the curve due to the bandwidth limitations of the tower. PTIs with better Bandwidth characteristics will have a sharper transition.

3. Propagation or Group delay: The length of time it takes the electromagnetic wave front to move through the interface. It is *related* to the overall length of the interface, but other factors combine to determine the final magnitude of this value. It can be seen on the graph as the horizontal distance between corresponding features of the waveform when comparing the Input and Output curves.

Frequency Response

Imagine standing at one end of a long hallway, and projecting a perfectly sung note down the hall (you do have perfect pitch, don't you?). There's a microphone right next to you, and another microphone at the far end of the hall. The ratio of the signal the microphone at the far end of the hall picks up, to the signal the microphone right next to you picks up, *as a function of the note you're singing* (the signal frequency), is the Frequency Response. At a given frequency, this ratio (usually expressed in decibels [dB]) will have a specific value, always with a magnitude less than 0 dB for a simple device like a PTI.

Measured using S (Scattering) - parameters, S_{21} and S_{12} measure how much of the signal which is sent to one side

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** Please note that some manufacturers show in their spec sheets a value of* (T_T) *or* (τ) *based on the time it takes the signal to swing from 20% to 80% of the full step. If your tester is in this group, you'll have to ask the manufacturer for the 10-90% numbers if you wish to use the equations at the end of the paper.*

of the PTI comes out the other side, as a function of frequency. "1" is the tester side and "2" is the probe card side of the interface.

S_{21} measures the ratio of the signal which arrives at the probe card side of the PTI to the signal sent to the tester side of the tower.

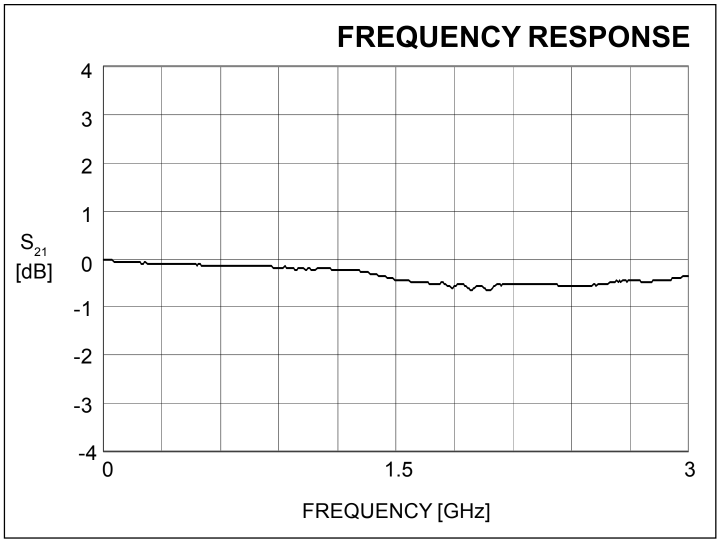
$$S_{21} = \frac{\text{Signal Transmitted to Port}_2}{\text{Signal Incident to Port}_1}$$

S_{12} measures the ratio of the signal which arrives at the tester side of the PTI to the signal sent to the probe card side of the PTI.

$$S_{12} = \frac{\text{Signal Transmitted to Port}_1}{\text{Signal Incident to Port}_2}$$

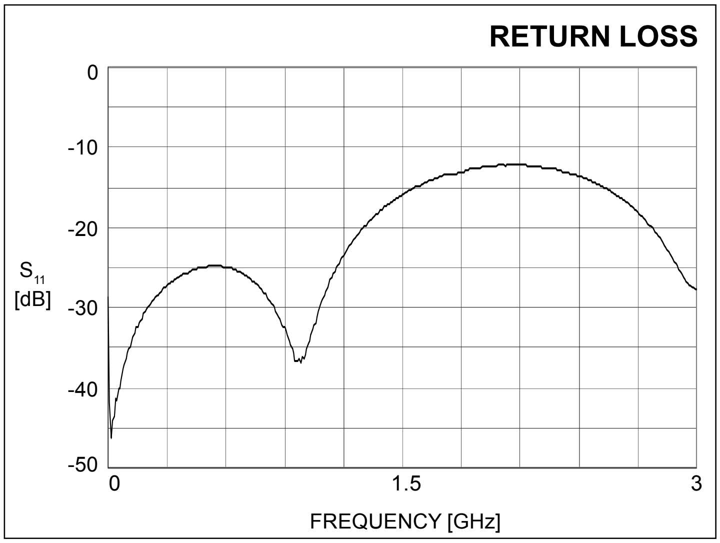
The resulting Frequency Response curves are also commonly called "Bandwidth" curves. Starting at the lowest possible frequency that the network analyzer can achieve (10 MHz or so), the frequency of a sine wave is swept up into the GHz range. The resulting plot shows the ratio of the strength of the injected signal to what comes out the other side, using a decibel scale on the vertical axis (typically 1 dB per division) and frequency on the horizontal axis.

Ideally the curve would go straight across the page along the 0 dB line (a Frequency Response of 1, or "unity"), with all of the signal passing through the tower with no loss, at all frequencies. The real world curve will tend downwards as one looks from left to right (from low to high frequencies).



Reflection Coefficient (Return Loss)

S_{11} and S_{22} measure the Reflection Coefficient, or Return Loss of the electrical system. Imagine standing at the end of that same hallway and singing that perfect note. There are two microphones again, but this time they're both right next to you. One is directly picking up the note you're singing, and the other is listening down the hall for any echo which might come back.



The Reflection Coefficient is a measure of how much of the signal sent to the PTI is reflected back at a given test frequency. The "far" end of the tower is terminated with an ideal load for this test. As you can see from the charts, this is also a frequency dependent function, with frequency on the horizontal axis and the ratio of the two signals (usually expressed in dB) on the vertical scale. If expressed in dB, the Reflection Coefficient is then called the "Return Loss."

S_{11} is the ratio of the signal reflected back to the tester to the original signal sent to the tester side of the PTI.

$$S_{11} = \frac{\text{Signal Reflected Back to Port}_1}{\text{Signal Incident to Port}_1}$$

S_{22} is the ratio of the signal reflected back to the probe card to the original signal sent to the probe card side of the PTI.

$$S_{22} = \frac{\text{Signal Reflected Back to Port}_2}{\text{Signal Incident to Port}_2}$$

The units on the vertical axis are typically 10 dB instead of the 1 dB per division used in the bandwidth curves.

The ideal situation would be for there to be no reflection at all (so the plotted line would start and end at around 40-to-50-dB-down, in the "noise floor" of the test equipment). As with the Frequency Response curves, a Reflection Coefficient of 1 is at the 0 dB Return Loss line. When the Return Loss is 0 dB, all of the signal sent to the PTI is reflected back to its source.

Putting All These Graphs and Numbers to Work

Determine the fastest Rise Time or Transition Time (τ or T_T) your tester's electronics are capable of. This can be found in the tester's specification sheets, or is certainly available from the manufacturer of the tester. The following chart will help you determine whether the PTI under consideration has a sufficiently fast Rise Time to meet your requirements:

$\frac{\tau_{\text{Tester}}}{\tau_{\text{PTI}}}$	τ degradation (%)
7	1
3.12	5
2.18	10
1.51	20
1	41

The formula for the table is as follows:

$$100 \text{ x} \left| \frac{\sqrt{(\tau_{\text{Tester}})^2 + (\tau_{\text{PTI}})^2}}{\tau_{\text{PTI}}} - 1 \right|$$

Determine what Bandwidth you need from the following equation:

$$\text{Bandwidth (in Hz)} = \frac{0.35}{\text{your tester's } \tau \text{ [in seconds]}}$$

For example, let's say that your tester is capable of creating signals with a rise time of 3.5 ns. The required Bandwidth of a PTI for your tester can be calculated thusly:

$$\frac{0.35}{3.5 \text{ x } 10^{-9} \text{ seconds}} = 1 \text{ x } 10^{8} \text{ Hz [100 MHz]}$$

Look at the Frequency Response S-parameter (**S_{12}**, **S_{21}**) graphs. At the Frequency determined in step 2, the signal loss must be negligible, certainly less than 1 dB.

Look at the Return Loss S-parameter (**S_{11}**, **S_{22}**) graphs. At *and* below the Frequency determined in step 2, the curve must be below the 20-dB-down line.

Other Considerations

You've probably noticed that at no time in this discussion was there any mention of the *PTI*'s impedence. Typical impedences for test systems will be 93, 75 or, most commonly, 50 ohms. The test head designer will establish the system's nominal impedence. The load board (or Prober Interface Board "PIB"), the PTI and the probe card must all be designed to match this chosen value as closely as they can. The better the match of each of these components, the better the curves will be. This is *not* to say that the way to get a good PTI is to just request that the manufacturer design to a particular impedence, to some extreme level of accuracy.

The important electrical values you need to share with the PTI designer are:

- Rise Time, or τ, of the test head
- The nominal impedence of the test head
- The maximum current and the maximum voltage delta (relative to the surrounding pins) any individual PTI pin could see, based upon the test capabilities of the test head, *not* the test programs currently being run! What's "good enough" today won't cut it tomorrow. So it's best to design to the test head's capabilities, rather than the challenges at hand.

The PTI engineer will optimize the design around *all* of these characteristics. Note that there was no mention of clock signal frequency. The test head's Rise Time is a much better indication of the highest frequency sinusoidal signal component the PTI must pass than the nominal clock frequency being sent to the DUT.

The PTI, with its highly regular pattern of ground and signal pins, is a *relatively* simple device. Controlling the impedence of the individual pins is a straightforward design task, and can be done to a high level of precision.

The designers of the load board and the probe card, however, have a much more daunting task. The extremely limited space which is available, as well as the requirement to route signals past each other in highly complex patterns, make it extremely difficult, if not impossible, for these parts to closely match the system's nominal impedence.

Once the signal has left the probe card and is headed down the tungsten needle to the DUT, controlled impedence is thrown to the wind. Not only is the free-hanging needle uncontrolled, but it is being terminated to a device, the DUT, which is almost certainly not a 50 ohm load.

There are design practices and probe card types which can minimize this problem, but they are expensive, add complexity and, consequently, are rarely used today. If the goal continues to be "at-speed" testing at wafer sort (and I suspect it will be), then these now unusual and costly techniques will have to be brought into play as test signal frequencies continue to increase.

The consequences of these mismatches are exactly what you'd expect: Reduced signal fidelity at wafer sort, relative to package sort. As it stands today, a well-designed PTI will be at least an order of magnitude better at signal transmission than the typical well-designed load board or probe card. Not for lack of trying on the part of the load board or probe card designer, but based upon the typical design practices which are used when creating these devices.

Finally, a well-designed PTI will not only deliver the electrical signal efficiently and with the least possible impact upon the transmitted signal, but will also have the following characteristics:

- Robust design, so as to survive the sort floor environment.
- Designed-in simplicity of repair, so the PTI can be quickly be returned to service after one of those rougher incidents which we all know happen on sort floors – happens.
- Ease-of-use, so that the operator will not be fighting with the PTI while trying to get their job done. To accomplish this, not only the PTI, but the Prober-to-PTI mechanical interface will most likely have to be redesigned as well.

I hope you have found this paper informative and useful. If you have any questions, or insights into any of the issues mentioned here which you'd care to share, please contact me. This is a "living" document which will be revised as new information becomes available.

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